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Characterization And Metrology Of Si/Si(1-X)Ge(X) Nanoscale Superlattice Film Stacks And Semiconductor Device Structures

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Extended Abstract

As traditional scaling of transistors comes to end, transistor channels and capacitors are being stacked to form new 3D transistor and memory devices. Many of these devices are fabricated using films stacks consisting of multiple Si/Si(1-x)Gex layers known as superlattices which must be fabricated with near atomic precision. The Si and Si(1-x)Gex layers in superlattice structures used for transistors are both < 10 nm thick while the 3D DRAM films are expected to be ~ 20 nm thick. In this talk, we discuss how optical, X-Ray, and electron microscopy methods are used to measure the feature shape and dimensions of these structures. The use of X-Ray methods such as ω-2θ scans and reciprocal space maps provide layer thickness, germanium concentration, and layer stress characterization. We will use simulations to show how a buried layer with a different thickness or Ge concentration alters the data. The differences between transistor and 3D DRAM superlattice characterization are highlighted. Recent electron microscopy studies have quantified the Si(1-x)Gex layer stress and the physical changes at the interfaces of few layer superlattices. We will also discuss how Mueller Matrix spectroscopic ellipsometry (MMSE) based scatterometry is used to measure feature shape and dimension for the nanowire/nanosheet structures used to fabricate nanosheet transistors and eventually 3D DRAM during manufacturing. The starting point for optical scatterometry is determining the optical properties of stressed pseudomorphic Si(1-x)Gex. MMSE can be extended into the infra-red and into the EUV. In addition, small angle X-Ray scattering has been adapted into a method knows as CDSAXS which can be used to characterize these structures. This talk will be an overview of these methods.